AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A method of forming a dual-sided semiconductor device from a wafer, the wafer having a first surface, an opposing second surface, and a dopant concentration, the method comprising the steps of:

forming a layer of masking material ~~on~~ over the first surface of the wafer;

patterning the layer of masking material to ~~expose~~ define a first region on the first surface; and

forming an opening in the wafer and a doped region in the wafer, the opening forming exposed regions of the wafer, the doped region having a first surface exposed by the opening in the wafer, ~~and~~ a dopant concentration that is greater than the dopant concentration of the wafer, and lying spaced apart from and between the first surface and the second surface of the wafer.

2. (Currently Amended) The method of claim 21 and further comprising the steps of:

forming a layer of masking material on the second surface of the wafer to expose a second region on the second surface of the wafer, the first and second regions being substantially vertically aligned,

forming an opening in the second surface of the wafer to expose the doped region in the wafer, the doped region having a second surface exposed by the opening in the second surface of the wafer; and

forming a layer of conductive material in the opening ~~to fill up the opening~~ in the second surface of the wafer ~~and~~ to form a second conductive region that contacts the doped region.

3. (Previously Amended) The method of claim 21 wherein the step of forming an opening in the wafer and a doped region in the wafer includes the steps of:

forming a layer of masking material on the second surface of the wafer to expose a second region on the second surface of the wafer, the first and second regions being substantially vertically aligned;

introducing a dopant into the wafer through the first and second regions, the dopant extending continuously through the wafer from the first region to the second region, and forming a continuous region through the wafer that has a dopant concentration greater than a dopant concentration of the wafer; and

etching the first and second regions for a predetermined period of time after the dopant has been introduced to define a first opening in the first surface of the wafer, a second opening in the second surface of the wafer, and the doped region there between.

4. (Previously Amended) The method of claim 21 wherein the step of forming an opening in the wafer and a doped region in the wafer includes the steps of:

forming a layer of masking material on the second surface of the wafer to expose a second region on the second surface of the wafer, the first and second regions being substantially vertically aligned;

introducing a dopant into the wafer through the first and second regions, the dopant extending continuously through the wafer from the first region to the second region;

removing the layer of masking material after the dopant has been introduced;

forming a protective layer on the first surface and the second surface of the wafer after the layer of masking material has been removed;

patterning the protective layer to expose the first region of the first surface, and the second region of the second surface; and

etching the first and second regions for a predetermined period of time after the protective layer has been patterned to define a first opening in the first surface of the wafer, a second opening in the second surface of the wafer, and the doped region there between.

5. (Currently Amended) ~~The method of claim 21 wherein the step of forming an opening in the wafer and a doped region in the wafer includes the steps of:~~ A method of forming a dual-sided semiconductor device from a wafer, the wafer having a first surface, an opposing second surface, and a dopant concentration, the method comprising the steps of:

forming a layer of masking material over the first surface of the wafer;

patterning the layer of masking material to define a first region on the first surface of the wafer;

forming a layer of masking material on the second surface of the wafer to expose a second region on the second surface of the wafer, the first and second regions being substantially vertically aligned;

etching the first and second regions for a predetermined period of time to define a first opening in the first surface of the wafer, a second opening in the second surface of the wafer, and a remaining region there between; ~~and~~

introducing a dopant into the wafer through the first and second openings, the dopant extending continuously through the remaining region to form the doped region, and having a dopant concentration that is greater than the dopant concentration of the wafer; and

forming a layer of conductive material in the first opening in the wafer to form a first conductive region that contacts the doped region.

6. (Previously Amended) The method of claim 21 wherein the step of forming an opening in the wafer and a doped region in the wafer includes the steps of:

forming a layer of masking material on the second surface of the wafer to expose a second region on the second surface of the wafer, the first and second regions being substantially vertically aligned;

etching the first and second regions for a predetermined period of time to define a first opening in the first surface of the wafer, a second opening in the second surface of the wafer, and a remaining region there between;

removing the layer of masking material after the etch has been completed;

forming a protective layer on the first surface and the second surface of the wafer after the layer of masking material has been removed;

patterning the protective layer to expose a top surface of the remaining region, and a bottom surface of the remaining region; and

introducing a dopant into the wafer through the first and second openings, the dopant extending continuously through the remaining region.

7. (Previously Amended) The method of claim 21 and further comprising the step of forming a diffusion barrier on the doped region and exposed regions of the wafer.

8. (Cancelled.)

9. (Original) The method of claim 2 and further comprising the step of forming a first device that contacts the first conductive region, and a second device that contacts the second conductive region.

10. (Currently Amended) ~~The method of claim 21 wherein the doped region has~~ A method of forming a dual-sided semiconductor device from a wafer, the wafer having a first surface, an opposing second surface, and a dopant concentration, the method comprising the steps of:

forming a layer of masking material over the first surface of the wafer;

patterning the layer of masking material to define a first region on the first surface;

forming an opening in the wafer and a doped region in the wafer, the opening forming exposed regions of the wafer, the doped region having a first surface exposed by the opening in the wafer, a dopant concentration that is greater than the dopant concentration of the wafer, and a second surface substantially planar with the second surface of the wafer, the first surface of the doped region and the second surface of the wafer being roughly parallel.

11. (Currently Amended) ~~The method of claim 10 wherein the step of forming an opening in the wafer and a doped region in the wafer includes the steps of:~~ A method of forming a dual-sided semiconductor device from a wafer, the wafer having a first surface, an opposing second surface, and a dopant concentration, the method comprising the steps of:

forming a layer of masking material over the first surface of the wafer;

patterning the layer of masking material to define a first region on the first surface;

introducing a dopant into the wafer through the first region, the dopant extending continuously through the wafer from the first surface of the wafer to the second surface of the wafer; and

etching the first region for a predetermined period of time after the dopant has been introduced to define ~~the~~ an opening in the wafer, and ~~the~~ a doped region between the opening and the second surface of the wafer, the doped region having

a surface substantially planar with the second surface of the wafer, and a dopant concentration that is greater than the dopant concentration of the wafer; and

forming a layer of conductive material in the first opening in the wafer to form a first conductive region that contacts the doped region.

12. (Currently Amended) ~~The method of claim 10 wherein the step of forming an opening in the wafer and a doped region in the wafer includes the steps of:~~ A method of forming a dual-sided semiconductor device from a wafer, the wafer having a first surface, an opposing second surface, and a dopant concentration, the method comprising the steps of:

forming a layer of masking material over the first surface of the wafer;

patterning the layer of masking material to define a first region on the first surface;

etching the first region for a predetermined period of time to define the opening in the wafer, and a remaining region between the opening and the second surface; ~~and~~

introducing a dopant into the wafer, the dopant extending continuously through the remaining region to form the doped region, the doped region having a surface substantially planar with the second surface of the wafer, and a dopant concentration that is greater than the dopant concentration of the wafer; and

forming a layer of conductive material in the first opening in the wafer to form a first conductive region that contacts the doped region.

13. (Currently Amended) ~~The method of claim 10 and further comprising the step of~~ A method of forming a dual-sided semiconductor device from a wafer, the wafer having a first surface, an opposing second surface, and a dopant concentration, the method comprising the steps of:

forming a layer of masking material over the first surface of the wafer;

patterning the layer of masking material to define a first region on the first surface;

forming an opening in the wafer and a doped region in the wafer, the opening forming exposed regions of the wafer, the doped region having a surface exposed by the opening in the wafer, a dopant concentration that is greater than the dopant concentration of the wafer, and a surface substantially planar with the second surface of the wafer;

forming a layer of conductive material in the opening in the wafer to form a first conductive region that contacts the doped region; and

forming a first device that contacts the first conductive region, and a second device that contacts the doped region.

14. (Currently Amended) The method of claim ~~10~~ 13 and further comprising the step of forming a contact through the doped region to make an electrical connection with the first conductive region.

15. (Original) The method of claim 14 and further comprising the step of forming a first device that contacts the first conductive region, and a second device that contacts the contact.

Claims 16-20 (Cancelled.)

21. (Currently Amended) The method of claim 1 and further comprising the step of forming a layer of conductive material in the opening to ~~fill up the opening in the wafer and~~ form a first conductive region that contacts the doped region.